Élan Am386SC300 Device Minimizing RAS Spikes During Page Access

Application Note

Advanced Micro Devices

Due to the switching characteristics of the memory interface within the Élan device, the RAS signal may spike during page accesses. When a page hit occurs, RAS remains active throughout the cycle, while the CAS and memory addresses (MA10-MA0) continue to switch to indicate a new column address within that page.

RAS SPIKE DURING PAGE ACCESS

During lab experiments with an ÉLAN Rev. 2.1 Evaluation board, spikes of up to 900 mV in amplitude and 5 ns in duration were captured on RAS during the transistion of the memory address. The memory interface was run at 5.0 V and the drive strength set at 16 mA during this experiment.

Follow these recommendations to minimize spikes:

- Run memory interface at 3.3 volts. This will require using 3.3-volt DRAM devices.
- Decrease the drive strengths for MA10-MA0 and MWE by modifying register at index B9. The default strength is 16 mA.
- Place series resistors on the RAS lines as close to the Élan device as possible.
- Place series resistors on MA10-MA0 as close to the Élan device as possible.

Issue Date: **September 1995**